fabricating a second output FET with a second plurality of interdigitated segments in a third area of the semiconductor die adjacent the first side of the control circuit, the second output FET having a length and a width, the length of the second output FET being substantially equal to the length of the control circuit, the width of the second output FET plus the width of the control circuit being substantially equal to the overall width of the semiconductor die;

coupling the first output FET to the gate terminal and the second output FET to the control circuit.

5. The method of claim **4** wherein the control circuit comprises a switched mode regulator control circuit.

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